

TEST PROGRAM DX-7

TEST PROGRAM OPERATION AND TROUBLE SHOOTING GUIDE

006557

SINCE 1887



YAMAHA

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1. TEST PROGRAM INTRODUCTION

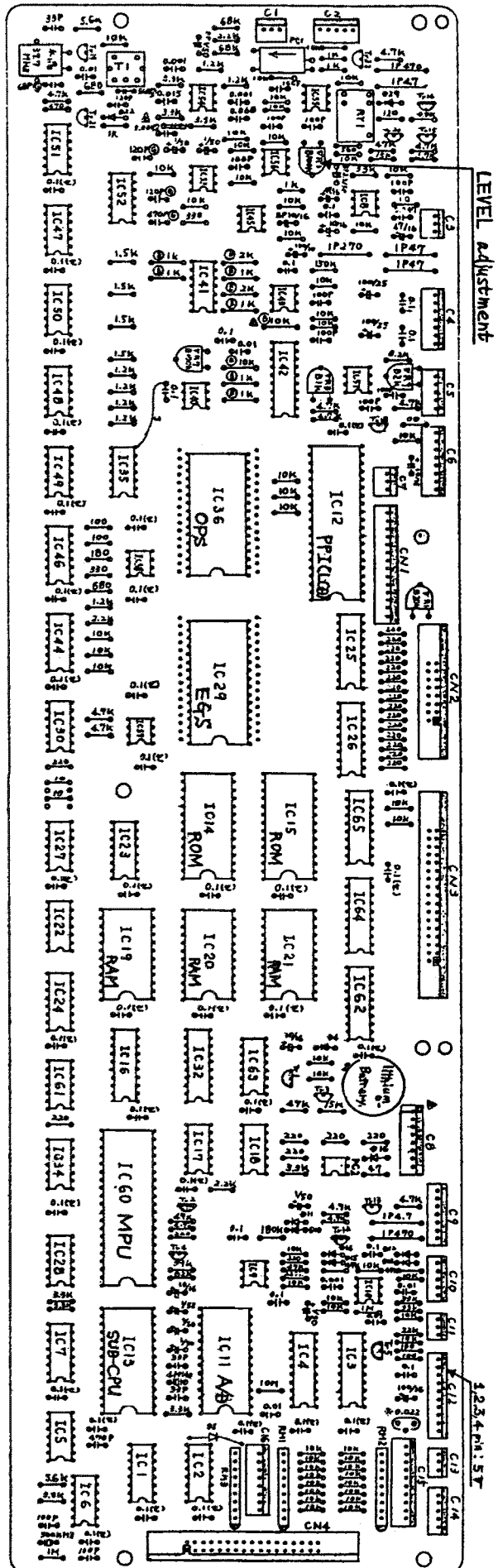
DX7 system control is handled by a microcomputer with specially designed software. Integrated circuits are of course used for the microcomputer's CPU and memory. Transfer, processing, and control of program data are carried out at high speed and it is thus difficult to analyze hardware failures using conventional procedures. Since the DX7 is program-controlled, however, function checks can be made with a test program, by simple operation of the control panel. This test program was developed to simplify checking for and locating system failure. The test program is already loaded together with the system program, so testing can be done by easily at the control panel. It should be noted, however, that the test program is not failure-proof. Since it depends on the power supply, clock, and CPU of the computer, it will not work when there is a fundamental failure in the microcomputer.

< FEATURES >

1. The test program is wired in, so it is possible to switch easily in and out of testing mode by operating a switch on the control panel.
2. Normal operation of the switches and volume control knobs can be confirmed by LED display.
3. RAM failure is indicated by display of corresponding IC number.

2. DX7 PARTS LAYOUT

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3. WHAT TO CHECK WHEN TEST PROGRAM FAILS

When the test program fails, check the following:

1) +5V

CN12	1, 2, 3, 4 pin
IC60 (MPU)	21 pin, 7 pin
IC14, 15 (ROM)	1 pin
IC19, 20, 21 (RAM)	24 pin
IC32, 17	20 pin
IC12 (PPI-LCD)	26 pin
IC25, 26 (LED)	20 pin

2) Clock

IC60 (MPU)	3 pin (ϕM)
IC13 (SUB-CPU)	5 pin (4 MHz)
IC29 (EGS)	63 pin, 64 pin ($\phi Ea, \beta$)
IC36 (OPS)	63 pin, 64 pin ($\phi Oa, \beta$)

3) RESET (Must be + 3.5V)

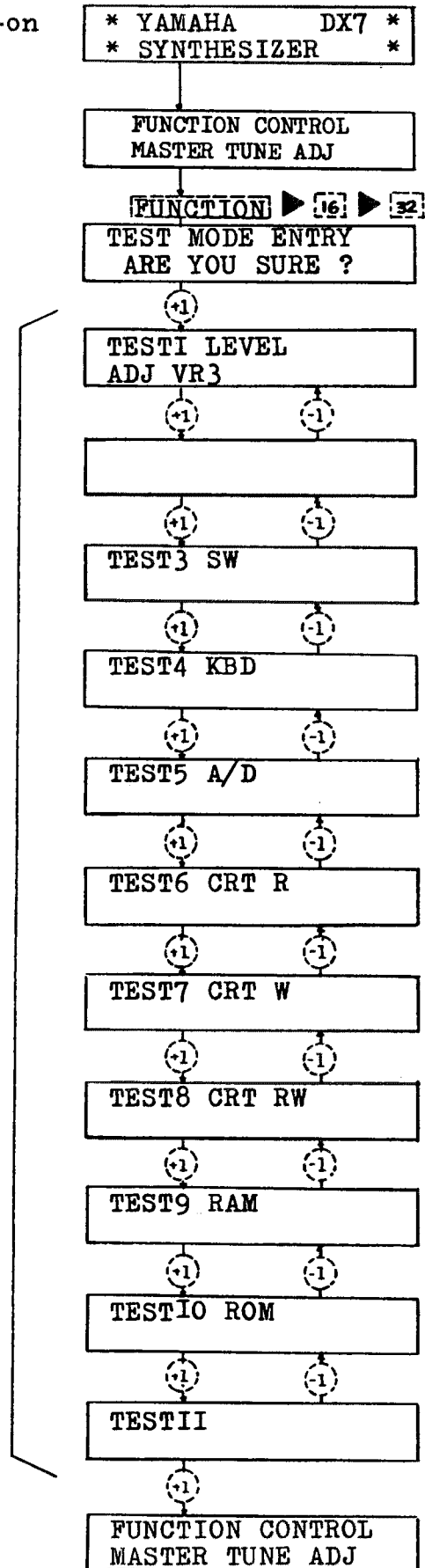
IC60 (MPU)	6 pin
IC13 (SUB-CPU)	28 pin

4) Address Bus, Data Bus

- When the program is running, all lines change irregularly between "H" and "L". Therefore, normality of operation can be judged with the synchroscope to some extent.
- Each line can be checked with a conductivity tester.

4. DX7 TEST ROUTINE

power-on



Keeping **Function** switch depressed, push switch **16** and then switch **32** to enter test mode.

Indicates that **+ 1** Yes switch should be pushed once.

Outputs sine wave (440 Hz A₃).

Indicates that **- 1** No switch should be pushed once.

LED and LCD flash.

Switch contact check.

Keyboard contact check.

A/D conversion, control volume knob check.

CARTRIDGE read check.

CARTRIDGE write (1 byte only) check.

CARTRIDGE read, write check.

RAM IC check.

ROM IC check.

Auto scaling from low note to high note.

5. TEST 1 LEVEL ADJUSTMENT

TEST 1 LEVEL ADJ VR 3

Sine wave A_3 (440 Hz) is output so level can be set and pitch confirmed. (When master VR is at maximum, -10 dBm is output at the terminal.)

TEST CONTENTS

- 1) Basic blocks of EGS and OPS ICs
- 2) DAC IC
- 3) Analog circuits

CHECKPOINTS

- This test is used to check for defects in circuits following the EGS/OPS.
- Unmodulated data for the sine wave A_3 (440 Hz) is input into the EGS/OPS from the ROM, and data for all ICs can be observed on the synchroscope (see waveforms on next page).

EGS (IC 29)

- EC_1-EC_{12} : Press key and confirm change in pulse width and waveform.
- KON: Press key and check to make sure that pulse width increases only for key that is pressed.
- F_1-F_{14} : Waveform changes for key that is pressed so change in pitch data can be confirmed.

OPS (IC 36)

- DA_1-D_{12} : Press key and check to make sure that pulse width increases only for key which is pressed.
- EC_1-EC_{12} : The waveform changes for the key which is pressed, so change in the envelope data can be confirmed.

DAC (IC 42)

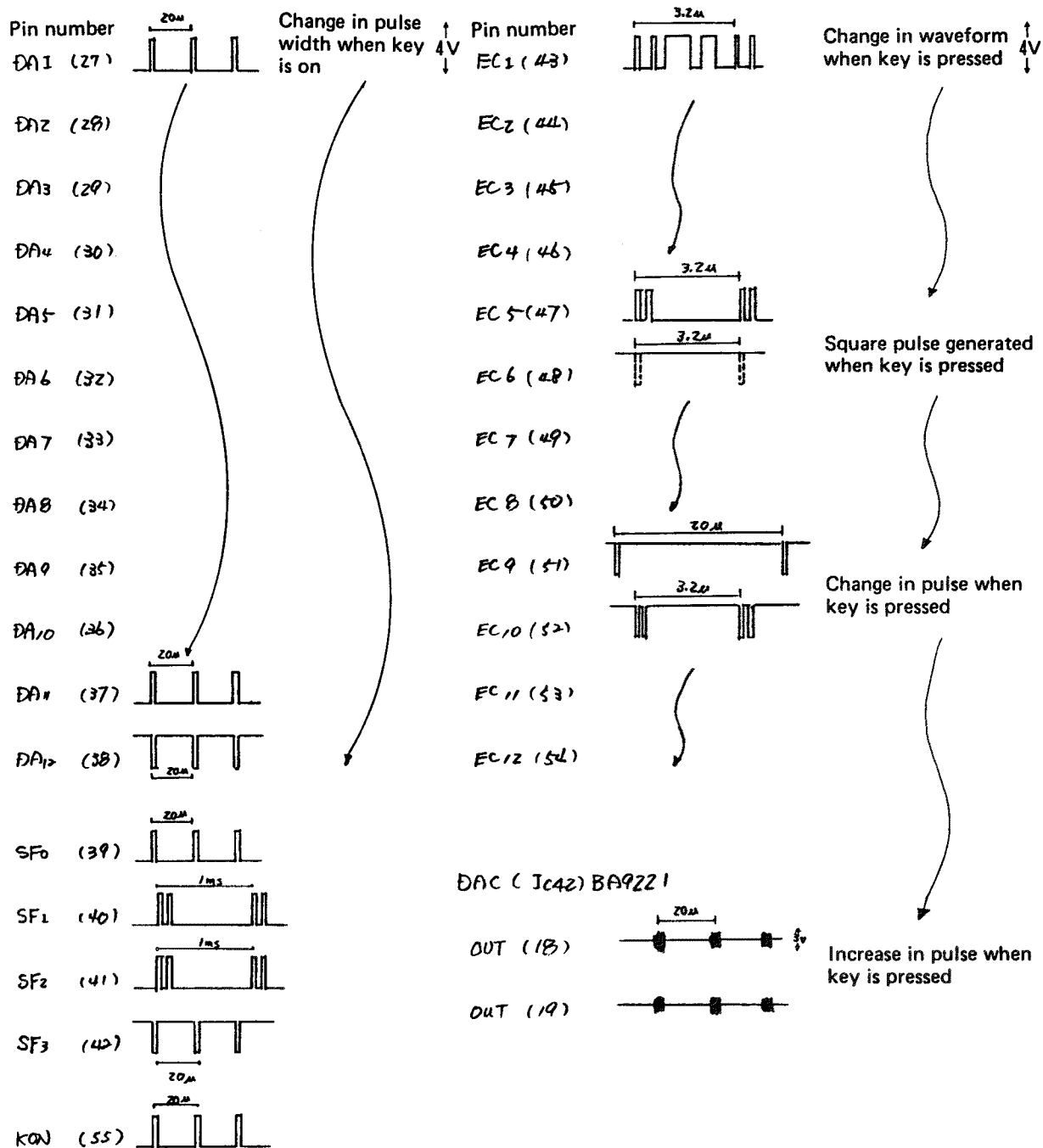
- Out waveform: Check to see that pulse is generated in a 20μ period. Press next keys and check to see that the pulse number increases.

LEVEL ADJUSTMENT

Adjust output level (master VR MAX) with VR3 B-100 K Ω to -10 dBm.

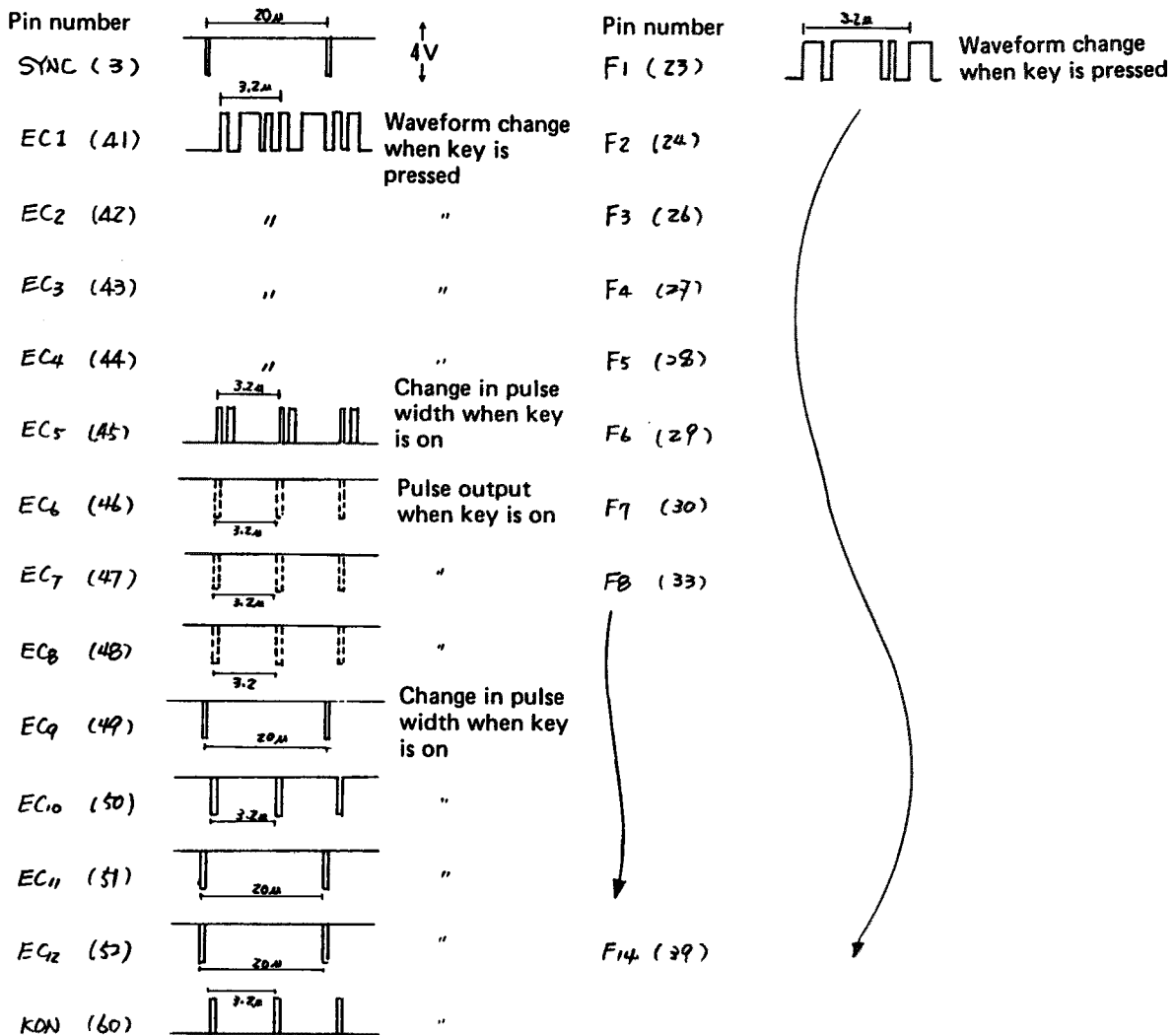
6. TEST 1 WAVEFORM

OPS (IC 36) YM 21280



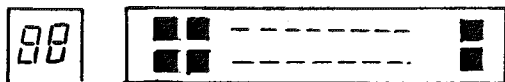
7. TEST 1 WAVEFORM DATA

EGS (IC 29) YM 21290



- Waveform of EC₁ ~ EC₄ and F₁ ~ F₁₄ changes when key is pressed.
- Pulse width of EC₅, EC₉ ~ KON increases according to the number of keys pressed.
- Pulse for EC₆ ~ EC₈ is output when key is pressed.

8. TEST 2 DISPLAY (LED AND LCD) TEST



The LED and LCD flash at 1 second intervals, so their condition can be evaluated visually.

TEST CONTENTS

- 1) Condition of LED unit
- 2) Condition of LED driver IC (ICs 25, 26)
- 3) Condition of LCD unit
- 4) Condition of LCD PPI (8255)

CHECKPOINTS

If LED doesn't light

Check to see if output terminals of IC25 and IC26 switch from "H" to "L" and back at 1 second intervals.

- If "H, L" pulse is present: Defect in LED unit or wiring
- If "H, C" pulse is not present: Defect in IC 25, 26

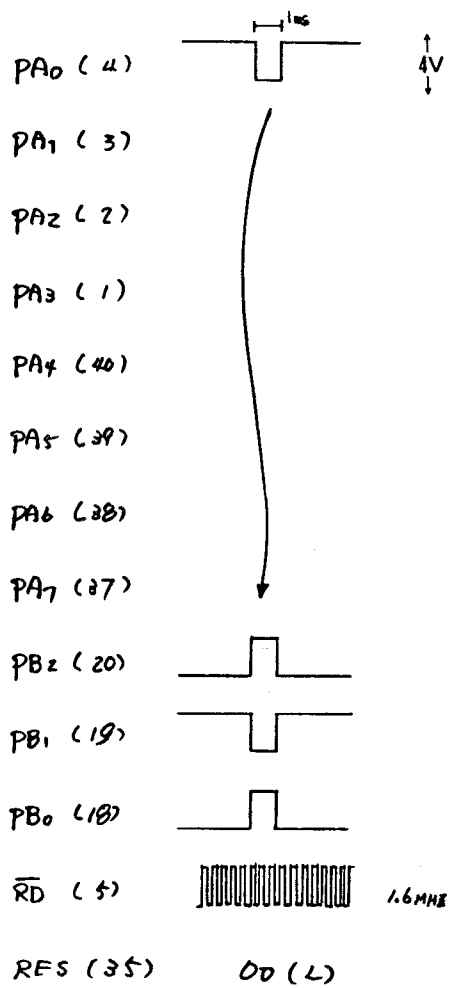
If LCD does not light, check the IC 12 (8255) data with the synchroscope.

- 1) PA0—PA7: Is 1ms pulse output?
- 2) PB0—PB1: Is 1ms pulse output?
- 3) RD terminal: Is clock output 1.6 MHz?
- 4) WR terminal: Is clock output 1.6 MHz?
- 5) CS terminal: Is IC 12 selected by chip select?

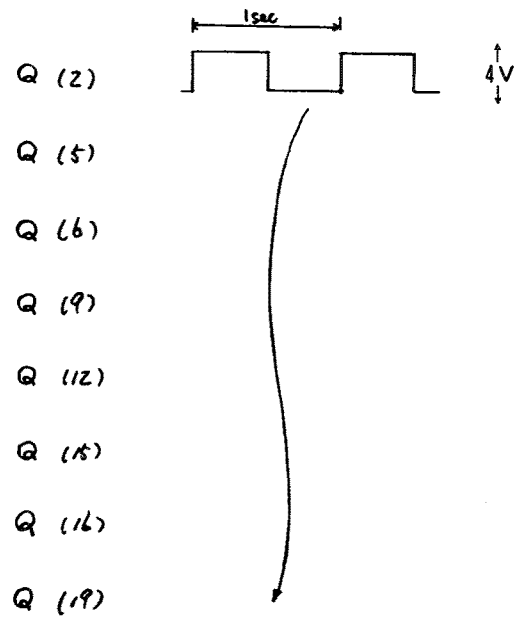
Refer to next page for correct form of data items 1) through 5) . If data is correct, a defect in the LED unit or wiring is indicated.

9. TEST 2

PPI (IC12) 8255



D F/F (IC26, 25)



Pulse generated by LED flashing speed

10. TEST 3

SWITCH CONTACT TEST

Test 3 SW

LED indicates 1. Press switches #1 through #40 as indicated by LED. From #33 on, the switch order is: STORE, INT, CRT, OPSEL, EDIT, INT, CRT, FUNCTION.

When all switches are normal, the display reads:

40	TEST 3 SW OK
----	-----------------

When a switch other than the one specified (e.g., #15) is pressed (e.g., #15) is pressed:

15	TEST 3 SW ERROR SEE LED
----	----------------------------

When a contact defect exists in a switch (e.g., #10), the number of the defective switch is displayed.

10	TEST 3 SW ERROR SEE LED
----	----------------------------

Test Contents

- 1) Condition of switch
- 2) Condition of SUB-CPU (IC13)
- 3) Condition of shift IC (IC1, 2)
- 4) Condition of buffer IC (IC3, 4)
- 5) Switch circuit connector, wiring check

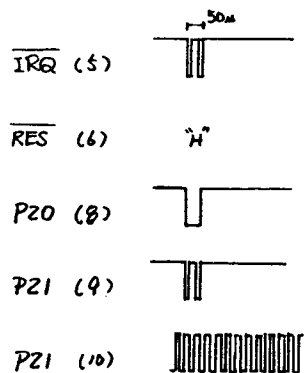
Checkpoints

Check the following items when a switch contact failure occurs.

- 1) When a switch is pressed, an IRQ (interrupt request) is always made from the sub-CPU (IC13) to the main CPU (IC60). Check the CPU (IC60) data on the synchroscope.
- 2) Check to see if multiplex data is output from the sub-CPU (IC13) to the switch.
- 3) The multiplex data referred to in item 2 is converted to Y5-Y7 data by IC12 (shift IC).
- 4) Check to see if data is input into buffer IC (IC4, 5) when switch is pressed.

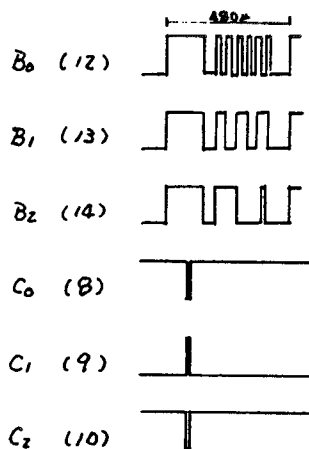
11. TEST 3 WAVEFORM

CPU (IC60) 63B03



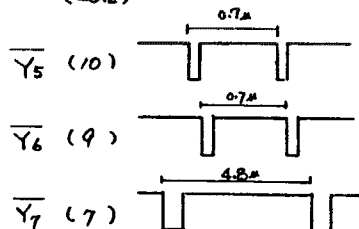
Pulse generated when switch is turned on and off. \uparrow 4V \downarrow

SUB-CPU (IC13) 6805S

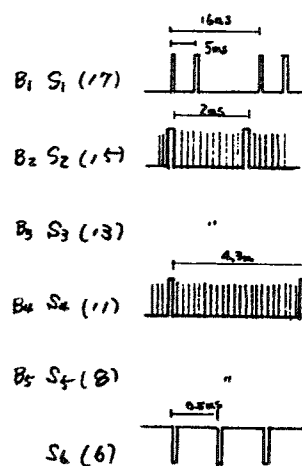


Pulse generated when switch is turned on and off.

(IC12)



(IC4)

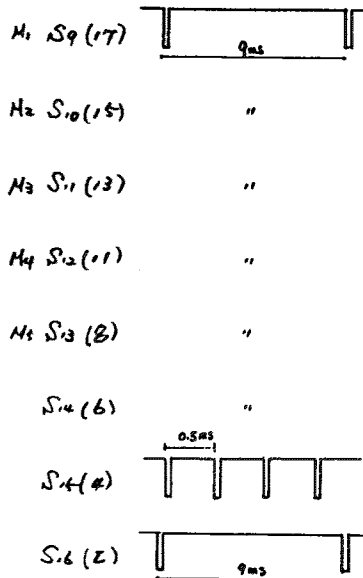


Pulse generated when switch is turned on. \uparrow 4V \downarrow

S_7 (4)

$PS S_8$ (2)

(IC5)



12. TEST 4 KEYBOARD CONTACT TEST

TEST 4 KBD

Key number is displayed on LED; pitch name is displayed on LCD. Press keys as indicated.

When all keys are normal, the display reads:

5 !	TEST 4 KBD KBD OK C6
-----	-------------------------

When a key other than the one indicated is pressed (e.g., the wrong key is pressed at sound 10):

1 0	TEST 4 KBD KBD ERROR A
-----	---------------------------

When a keyboard switch contact failure exists (e.g., at sound 15):

1 5	TEST 4 KBD KBD ERROR D
-----	---------------------------

Test Contents

- 1) Condition of keyboard switch contact
- 2) Sub-CPU (IC13)
- 3) Data IC (IC1, 2)
- 4) Buffer IC (IC3, 4)
- 5) Condition of wiring, connectors

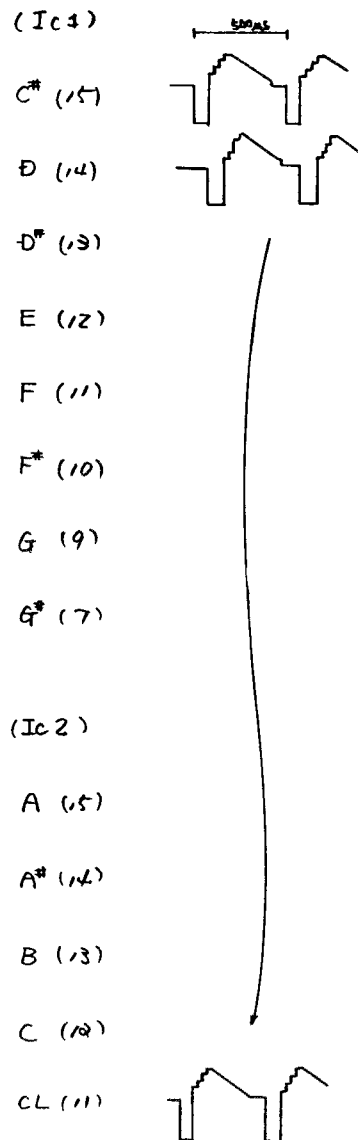
Checkpoints

- 1) As in test 3, check the waveform when key is pressed to make sure that an IRQ (interrupt request) is made from SUB-CPU to Main-CPU.
- 2) Make sure that all note data is shifted in order in IC1 and IC2 and that pulse is output.
- 3) Make sure that pulse is output for IC4 (Break data) and IC5 (Make data) when key is pressed.

Checkpoints

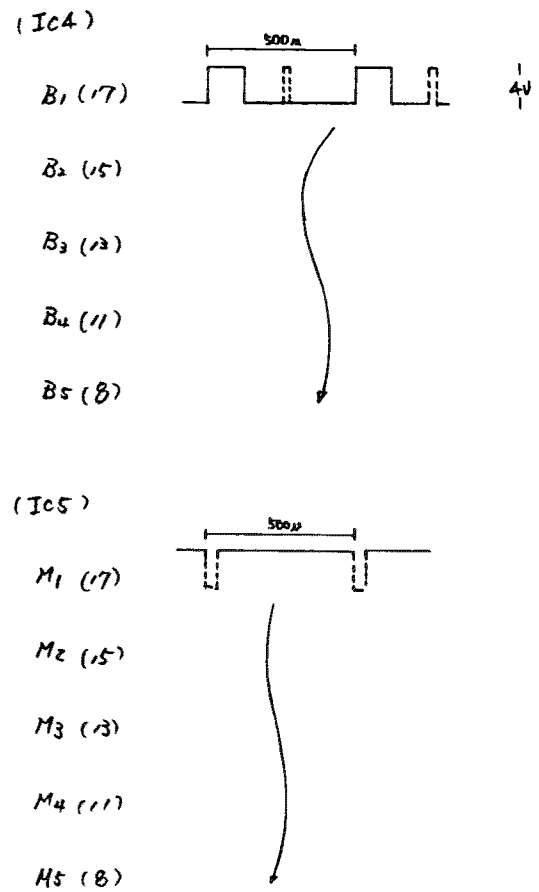
- 1) As in test 3, check the waveform when key is pressed to make sure that an IRQ (interrupt request) is made from SUB-CPU to Main-CPU.

13. TEST 4 WAVEFORME



4V

Minus pulse
is shifted.



4V

Break (B₁ ~ B₅)

Make (M₁ ~ M₅)

When a key is pressed in each OCT, a pulse
(dotted line) is generated with a period of
500μs.

14. TEST 5 A/D

TEST 5 A/D

The input levels of analog data are displayed in numbers from 1 to 99 on LED. A check can be made to confirm that all analog data has been correctly digitized.

Test Contents

- 1) Condition of all volume.
- 2) Condition of all buffer ICs.
- 3) Condition of A/D IC (IC11, M85990)

Checkpoints

Input terminal (IC11)

DATA ENTRY	IN ₀ (26)
PITCH BEND	IN ₁ (27)
MODULATION WHEEL	IN ₂ (28)
FOOT CONTROL	IN ₃ (1)
BREATH CONTROL	IN ₄ (2)
AFTER TOUCH		IN ₅ (3)

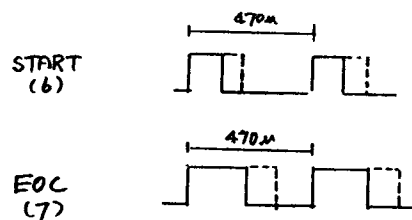
Output terminal (IC11)

A₀ (17) ~ A₇ (21)



Check for change in waveform as each analog data is changed.

IC11



Check to make sure that waveform changes as indicated by dotted lines when analog data is changed.

15. TEST 6 CARTRIDGE READ TEST

TEST 6 CRT R

First, enter specified data in CARTRIDGE memory. Add these data, compare with data in ROM, and check to see if CARTRIDGE reading is being performed correctly.

Normal:

TEST 6 CRT R
OK EEPROM

Error:

TEST 6 CRT R
ERROR EEPROM

Test Contents

- 1) Condition of CARTRIDGE (EPRAM)
- 2) Condition of buffer IC

16. TEST 7 CARTRIDGE WRITE TEST

TEST 7 CRT W

Insert CARTRIDGE with memory protect removed to perform this test. There are two EPROMs in the CARTRIDGE. Write and read one byte for each memory to check the condition of the CARTRIDGE.

Normal:

TEST 7 CRT W
WRITE OK

Error:

TEST 7 CRT W
WRITE ERROR

Test Contents

- 1) Checking condition of CARTRIDGE (EEPROM)
- 2) Checking condition of buffer IC

17. TEST 8 CARTRIDGE READ/WRITE TEST

TEST 8 CRT RW

By writing data into the CARTRIDGE and making a comparison with the original data, a check is made to determine whether reading and writing of data into and out of the CARTRIDGE is being performed correctly.

Press switch #1 to start the test.

During read/write execution:
(about 1 min.)

TEST 8 CRT RW
JUST CHECK

CRT OK:

TEST 8 CRT RW
EEPROM OK

CRT ERROR:

TEST 8 CRT RW
EEPROM ERROR

CRT WRITE ERROR:

TEST 8 CRT RW
WRITE ERROR

Test Contents

- 1) Condition of cartridge unit
- 2) Condition of Buffer IC
- 1) Condition of cartridge unit
- 2) Condition of Buffer IC

18. TEST 9 RAM TEST

TEST 9 RAM

By writing data into RAM and comparing it with original data, a check is made to determine whether writing into and reading out of RAM is performed correctly.

Press switch #1 to start test.

(Be sure to insert CARTRIDGE with write protect removed)

During WRITE execution:

TEST 9 RAM
UNDER WRITING

RAM OK:

TEST 9 RAM
RAM OK

RAM ERROR:

TEST 9 RAM
RAM ERROR

Test Contents

- 1) Condition of RAM IC
- 2) Condition of address decoder IC

Checkpoints

Check the following items when a RAM error occurs.

\overline{WE}  $4V$ $1.6\mu Hz$

$\overline{CE1}$  Pulse generated when RAM is active.

$\overline{CE2}$ $L (00)$

If the above items are correct, the RAM IC is defective.

19. TEST 10 ROM TEST (CHECK SUM)

TEST 10 ROM

All data in ROM is added and compared to previously computed data to check condition of ROM.

Normal ROM:

TEST 10 ROM
SUM CHECK OK

ROM Error:

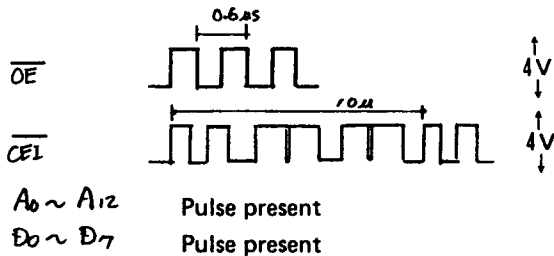
TEST 10 ROM
SUM CHECK ERROR

Test Contents

- 1) Condition of ROM
- 2) Condition of address decoder IC

Checkpoints

Check the following items when an error occurs:



When the data shown above are correct, the ROM is defective.